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DESCRIPTION

RADIO COMMUNICATION APPARATUS AND CODING PROCESSING METHOD

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This application is a 371 of PCT/JP00/01755 dated on March 23, 2000.
5 Technical Field

The present invention relates to a radio communication apparatus and a coding processing method employed in mobile radio communication.

10 Background Art

In mobile radio communication, particularly in CDMA radio communication, Rate matching processing is performed in order to enhance an effect of error correction, and/or in order to transmit data such as a packet, ISDN and so forth while coupling the data. The Rate matching processing is repetition processing for increasing the number of bits of data in order to adjust coded data to frame length, or puncturing processing for reducing the number of bits of data in order to adjust coded data to frame length. For instance, in a transmitter side, in the case where the transmitter side causes the number of bits of data to be increased, in a receiver side, the receiver side is required to perform processing of decreasing of the number of bits of data.

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25 In this case, since the transmitter side performs repetition, it is possible to increase a transmission power.

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FIG. 1A is a block diagram illustrating a configuration of a conventional coding processing apparatus in the case where repetition is performed in a transmitter side. Also, FIG. 1B is a block diagram illustrating a configuration of a conventional decoding processing apparatus in the case where repetition is performed in a transmitter side.

The coding processing apparatus 1 includes a coder 2, an error correction coder 3, a repetition section 3, and an interleaving section 5. The decoding processing apparatus 10 includes a deinterleaving section 11, a puncturing section 12, an error correction decoder 13, and a decoder 14.

In the transmitter side, transmitted data 6 is coded in the coder 2. This coded data is subjected to error correction coding processing such as convolutional coding and so forth in the error correction coder 3 before the number of bits is increased in the repetition section 4. The data after repetition is rearranged in the interleaving section 5. Subsequently, the data is subjected to predetermined modulation processing and radio processing and so forth, before being transmitted from a transmission antenna 7.

On the other hand, in the receiver side, a signal received by a reception antenna 15 is subjected to predetermined radio processing and demodulation processing and so forth before inverse rearrangement

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against the interleaving is performed in the deinterleaving section 11. In this rearranged data, the number of bits which are increased in the transmitter side once are decreased in the puncturing section 12.

5 The data is subjected to error correction by Viterbi decoding and so forth in the error correction decoder 13. This data after error correcting is decoded in the decoder 14. According to the above processing, received data 16 is obtained.

10 FIG. 2 is a view showing data arrangement in the case where repetition is performed with the conventional coding processing apparatus employed. Now, data outputted from the coder 2 is taken to be {D1, D2, D3, D4}. The data is subjected to error correction coding
15 processing with "code rate = 1/2" in the error correction coder 3. As a result, in cases where D1 becomes d1 and d2, D2 becomes d3 and d4, D3 becomes d5 and d6, and D4 becomes d7 and d8, data inputted to the repetition section 4 becomes data of 8 bits of {d1, d2, d3, d4, d5, d6, d7, d8}.
20 Further, the number of bits per 1 frame is set to 12 bits.

The repetition section 4 is provided with a Rate matching table. Further, a pattern of "0 and 1" is stored in the Rate matching table. The pattern of "0 and 1"
25 causes a distribution of increase of bits within a frame to be even. Now, if the Rate matching table is taken to be {1, 0, 1, 0, 1, 0, 1, 0}, since bits corresponding

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to "1" are increased, thus d1, d3, d5, and d7 showed by under lines are increased.

Accordingly, data after repetition becomes {d1, d1, d2, d3, d3, d4, d5, d5, d6, d7, d7, d8}. Careful
5 observation of the data after repetition reveals that there exist two increased bits and one not increased bit within continuous three bits, thus it is found that a distribution of increase of bits becomes even within a frame.

10 The data after repetition is subjected to interleaving in accordance with for instance an interleaving pattern ; $12[4[2 \times 2] \times 3[2 \times 2]]$. According to this processing, the data after interleaving becomes {d1, d5, d3, d7, d2, d6, d4, d8, d1, d5, d3, d7}.

15 According to these processing, it is possible to avoid a burst error in a propagation path in some degrees. Accordingly, it is possible to improve bit error rate characteristic in some degrees when the receiver side corrects errors.

20 However, in the above-described conventional coding processing apparatus, the increased bits caused by repetition are partial to a position within a frame according to an interleaving pattern. For this reason, an effect of the repetition deteriorates remarkably.

25 Consequently, the bit error rate characteristic deteriorates when the receiver side corrects errors.

Specifically, for instance, in an interleaving

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pattern showed in FIG. 2, increased bits "d1, d3, d5, d7" are partial to both sides within the frame. Accordingly, in the case where a burst error occurs in a propagation path at portions with not-increased bits "d2, d4, d6, d8", the bit error rate characteristic deteriorates when the receiver side corrects errors.

Disclosure of Invention

An object of the present invention is to provide a radio communication apparatus and a coding processing method in which resistibility to a burst error in a propagation path is high, and the apparatus and method are capable of scheming improvement of communication quality.

The inventor of the present invention notes a cause why the increased bits due to the repetition are partial to a portion within a frame. In the case where the repetition is performed at a time about the whole data before interleaving, the increased bits due to the repetition are partial to a portion within the frame. The inventor finds that the repetition is separated to be performed before and after interleaving in well-balanced condition, so that it is possible to prevent maldistribution of the increased bits due to the repetition within the frame, and the inventor achieves the present invention.

Accordingly, in order to achieve the above-

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described object, in the present invention, roughly half the number of bits increased due to the repetition are increased in accordance with a repetition before interleaving, while remaining the number of bits increased due to the repetition are increased in accordance with a repetition after interleaving.

Brief Description of Drawings

FIG. 1A is a block diagram illustrating a configuration of a conventional coding processing apparatus;

FIG. 1B is a block diagram illustrating a configuration of a conventional decoding processing apparatus;

FIG. 2 is a view showing data arrangement in the case where repetition is performed with the conventional coding processing apparatus employed;

FIG. 3A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 1 of the present invention;

FIG. 3B is a block diagram illustrating a configuration of a decoding processing apparatus according to an embodiment 1 of the present invention;

FIG. 4 is a block diagram illustrating a configuration of a repetition section and a puncturing section according to the embodiment 1 of the present invention;

FIG. 5 is a flowchart for explaining operation of

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a first repetition section according to the embodiment 1 of the present invention;

Fig. 6 is a flowchart for explaining operation of a second repetition section according to the embodiment 1 of the present invention;

FIG. 7 is a flowchart for explaining operation of a first puncturing section according to the embodiment 1 of the present invention;

FIG. 8 is a flowchart for explaining operation of a second puncturing section according to the embodiment 1 of the present invention;

FIG. 9 is a view showing data arrangement in the case where repetition is performed with the coding processing apparatus employed according to the embodiment 1 of the present invention;

FIG. 10A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 2 of the present invention;

FIG. 10B is a block diagram illustrating a configuration of a decoding processing apparatus according to the embodiment 2 of the present invention;

FIG. 11A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 3 of the present invention; and

FIG. 11B is a block diagram illustrating a configuration of a decoding processing apparatus according to the embodiment 3 of the present invention.

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Best Mode for Carrying Out the Invention

Embodiments of the present invention are explained in detail below with reference to accompanying drawings.

5 (Embodiment 1)

FIG. 3A is a block diagram illustrating a configuration of a coding processing apparatus according to the embodiment 1 of the present invention. Further, FIG. 3B is a block diagram illustrating a configuration of a decoding processing apparatus according to the embodiment 1 of the present invention. A coding processing apparatus 100 includes a coder 101, an error correction coder 102, a first repetition section 103, an interleaving section 104, and a second repetition section 105. In the meantime, a decoding processing apparatus 110 includes a first puncturing section 111, a deinterleaving section 112, a second puncturing section 113, an error correction decoder 114, and a decoder 115.

20 In the transmitter side, transmitted data 106 is coded in the coder 101. The coded data is subjected to error correction coding processing such as convolutional coding and so forth in the error correction coder 102, before being outputted to the first repetition section 103. The data after error correction coding processing is subjected to a first repetition as describe later in the first repetition section 103. The data after the

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first repetition is rearranged in the interleaving section 104, before being subjected to a second repetition as describe later in the second repetition section 105. The data after the second repetition is
5 subjected to predetermined modulation processing and predetermined radio processing and so forth thereafter. Then the data is transmitted from a transmission antenna 107.

On the other hand, in the receiver side, a signal
10 received by a reception antenna 116 is subjected to predetermined radio processing and predetermined demodulation processing and so forth. The data after predetermined radio processing and predetermined demodulation processing is subjected to a first
15 puncturing which is inverse processing against the second repetition in the first puncturing section 111. The data after the first puncturing is subjected to an inverse rearrangement against the interleaving in the transmitter side in the deinterleaving section 112.
20 This rearranged data is subjected to a second puncturing which is inverse processing against the first repetition in the second puncturing section 113. The data after the second puncturing is subjected to error correction by Viterbi decoding and so forth in the error correction
25 decoder 114, before being decoded in the decoder 115. According to the above processing, received data 117 is obtained.

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Next, there will be described about configuration of the first repetition section 103 while employing the block diagram illustrated in FIG. 4. In the first repetition section 103, an input memory 201 temporary
5 stores therein data being subjected to error correction coding. A parameter storage section 202 stores therein various kinds of parameters necessary for performing repetition. A controller 203 outputs a control signal for performing read/write of data to a memory read/write
10 section 204 on the basis of various kinds of parameters stored in the parameter storage section 202. The memory read/write section 204 reads the data from the input memory 201 successively, and outputs the data while increasing the number of bits to be targeted bits to an
15 output memory 205 on the basis of the control signal. The output memory 205 stores the data outputted successively from the memory read/write section 204 up to the state where the data for one frame is completed. Then the output memory 205 outputs the data for one frame
20 at the time when the data for one frame is completed.

Further, a configuration of the second repetition section 105 is roughly the same as that of the first repetition section 103. Accordingly, concerning the second repetition section 105, an explanation about the
25 configuration is omitted. There will be explained about only operation in an operation explanation describe later. Furthermore, also configurations of the first

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Next, in ST303, the controller 203 calculates a

first repetition interval 'X1' that means whether the controller 203 performs the first repetition in every how many bits in accordance with an expression (3).

$$X1 = N0/r1 \text{ (rounding off less than a decimal point)} \quad (3)$$

Next, in ST304, the controller 203 performs compensation of 'r1', and 'X1'. This compensation is one causing the first repetition to be executed in accordance with a code rate to be performed according to expressions (4) to (6). Specifically, for instance, in the case where a code rate of data is 1/2, the first repetition is performed in every the number of bits to be multiples of 2, while in the case where a code rate of data is 1/3, the first repetition is performed in every the number of bits to be multiples of 3. Thus 'r1' and 'X1' are compensated in accordance with above described manner.

Firstly, the controller 203 performs the remainder calculation showed in an expression (4).

$$\text{mod}(X1 + m, C) = 0 \quad m \geq 0 \quad (4)$$

Here, 'C' is an inverse number of a code rate of data, and this expression (4) is one for calculating the minimum 'm' causing the remainder to be '0' (zero) when 'X1+m' is divided by 'C'. The controller 203 calculates a compensated value 'X1'' of 'X1' in accordance with an expression (5) while employing 'm' calculated by this expression (4). According to this processing, 'X1' is compensated into 'X1''.

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$$X1' = X1 + m \quad (5)$$

Further, the controller 203 calculates compensated value 'r1'' of 'r1' in accordance with an expression (6) while employing 'X1'' calculated by the expression (5).
 5 According to this processing, 'r1' is compensated into 'r1''.

$$r1' = N0/X1' \quad (\text{rounding off less than decimal point}) \quad (6)$$

Subsequently, a value of a counter 'Ct' set in the
 10 controller 203 is added one by one from '1' (one). Then, processing of ST305 to ST310 is performed repeatedly over 'N0' times up to the state where the value of the counter 'Ct' becomes 'N0'. In ST306, the controller 203 performs the remainder calculation of an expression (7).

$$15 \quad \text{mod}(Ct, X1') = b1 \quad (7)$$

Here, 'b1' is a parameter for setting whether the first repetition is started from how many numbers of bits of a frame. The 'b1' is set in the parameter storage section 202 beforehand.

20 In ST306, in the case where the remainder of the division of dividing 'Ct' by 'X1'' becomes equal to 'b1', in ST307, the controller 203 sets the number of times 'n' of data output to '2'. in ST306, in the case where the remainder of the division of dividing 'Ct' by 'X1''
 25 does not become equal to 'b1', in ST308, the controller 203 sets the number of times 'n' of data output to '1'.

In ST309, the memory read/write section 204 reads

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5 According to a processing-flow described-above,
the first repetition of causing the number of bits to
be increased for only the number of bits 'r1'' roughly
half the number of total bits 'R' for the repetition is
performed. Concerning the data after the first
0 repetition, rearrangement of data is performed in
accordance with the interleaving pattern in the
interleaving section 104, subsequently the data is
subjected to the second repetition in the second
repetition section 105.

20 Firstly, in ST401, the controller 203 within the second
repetition section 105 calculates the number of bits 'r2'
for the second repetition in accordance with an
expression (8) from the number of total bits 'R' for the
repetition calculated by the first repetition section
103 and compensated number of bits 'r1' for the first
25 repetition.

Next, in ST402, the controller 203 calculates a

second repetition interval 'X2' that means whether the controller 203 performs the second repetition in every how many bits in accordance with an expression (9).

$$X2 = N1/r2 \text{ (rounding off less than a decimal point)} \quad (9)$$

Here, 'N1' is 'N1 = N0 + r1', which represents the number of bits after the first repetition.

Subsequently, a value of the counter 'Ct' set in the controller 203 is added one by one from '1'(one). Then, processing of ST403 to ST408 is performed repeatedly over 'N1' times up to the state where the value of the counter 'Ct' becomes 'N1'. In ST404, the controller 203 performs the remainder calculation of an expression (10).

$$\text{mod}(Ct, X2) = b2 \quad (10)$$

Here, 'b2' is a parameter for setting whether the second repetition is started from how many numbers of bits of a frame. This 'b2' is set in the parameter storage section 202 beforehand.

In ST404, in the case where the remainder of the division of dividing 'Ct' by 'X2' becomes equal to 'b2', in ST405, the controller 203 sets the number of times 'n' of data output to '2'. While, in ST404, in the case where the remainder of the division of dividing 'Ct' by 'X2' does not become equal to 'b2', in ST406, the controller 203 sets the number of times 'n' of data output to '1'.

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202 in accordance with control data transmitted from the transmitter side. This 'X2' is equal to the second repetition interval 'X2'.

Subsequently, the processing of ST502 to ST505 is performed repeatedly over 'N' times up to the state where a value of the counter 'Ct' set in the controller 203 is added one by one from '1' (one) to come into 'N'. Here, 'N' is ' $N = N0 + r1 + r2$ ', thus representing the number of bits after the second repetition, namely representing the number of bits per one frame. In ST503, the controller 203 performs the remainder calculation of an expression (11).

$$\text{mod}(Ct, X2) = b2 \quad (11)$$

Here, 'b2' is equal to 'b2' which is employed when the second repetition is performed. The 'b2' is set to the parameter storage section 202 in accordance with the above control signal.

Next, in ST504, the memory read/write section 204 reads data stored in the input memory 201 one bit by one bit. Then, in the case where the remainder of the division of dividing 'Ct' by 'X2' does not become equal to 'b2', the memory read/write section 204 writes the read data to the output memory 205 once. While in the case where the remainder of the division of dividing 'Ct' by 'X2' becomes equal to 'b2', the memory read/write section 204 abolishes the read data.

According to the processing-flow described-above,

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In ST603, the controller 203 performs the remainder

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calculation of an expression (12).

$$\text{mod}(\text{Ct}, \text{Xl}') = \text{b1} \quad (12)$$

Here, 'b1' is equal to the 'b1' employed when the first repetition is performed, to be set to the parameter storage section 202 in accordance with the above control signal.

Next, in ST604, the memory read/write section 204 reads the data stored in the input memory 201 one bit by one bit. Then in the case where the remainder of the division of dividing 'Ct' by 'Xl'' does not become equal to 'b1', the memory read/write section 204 writes the read data to the output memory 205 once. While in the case where the remainder of the division of dividing 'Ct' by 'Xl'' becomes equal to 'b2', the memory read/write section 204 abolishes the read data.

According to the processing-flow described-above, the second puncturing is performed to the bits increased by the first repetition. The data after the second puncturing is subjected to error correction by Viterbi decoding and so forth in the error correction decoder 114, before being decoded in the decoder 115. According to this processing, received data 117 is obtained.

Next, there will be described the circumstances in detail in which transmitted data is subjected to repetition and interleaving due to the coding processing apparatus 100 of the present embodiment while employing FIG. 9.

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Now, data outputted from the coder 101 is taken to be {D1, D2, D3, D4}. The data is subjected to error correction coding processing with "code rate = 1/2" in the error correction coder 102. As a result, in cases where 'D1' becomes 'd1', and 'd2', 'D2' becomes 'd3', and 'd4', 'D3' becomes 'd5', and 'd6', and 'D4' becomes 'd7', and 'd8', data inputted to the first repetition section 103 becomes data of 8 bits of {d1, d2, d3, d4, d5, d6, d7, d8}. Further, the number of bits per one frame is 12 bits.

In the first place, the first repetition section 103 performs the first repetition in accordance with processing-flow of FIG. 5. Firstly, in ST301 to ST303, 'R', 'r1', and 'X1' are calculated in accordance with above expressions (1) to (3). Following result is obtained.

$$R = N - N0 = 12 - 8 = 4 \quad (13)$$

$$r1 = R/2 = 4/2 = 2 \quad (14)$$

$$X1 = N0/r1 = 8/2 = 4 \quad (15)$$

Next, in ST304, 'r1' and 'X1' are compensated in accordance with above expressions (4) to (6). Now, since the code rate of the error correction coding processing is '1/2', 'C' becomes 'C=2'. Consequently, above expression (4) is calculated as following way.

$$\text{mod}(X1 + m, C) = 0$$

$$\text{mod}(4 + m, 2) = 0$$

$$\therefore m = 0 \quad (16)$$

Here, since 'm' is 'm=0', following result is obtained in accordance with above expressions (5), and (6).

$$X1' = X1 = 4 \quad (17)$$

$$5 \quad r1' = r1 = 2 \quad (18)$$

Next, in ST305 to ST310, the number of bits of corresponding bits is increased in accordance with the above expression (7) up to the state where 'Ct' becomes 'N0' from '1'. Now, in the case where 'b1' is set to "b1=2", in accordance with the above expression (7), the number of bits of 'd2' to be data of the second bit as well as the number of bits of 'd6' to be data of the sixth bit are increased, thus the first repetition is performed. Consequently, the data after the first repetition becomes {d1, d2, d2, d3, d4, d5, d6, d6, d7, d8} as showed in FIG. 9. Further, the data showed by underline in FIG. 9 are ones whose number of bits is increased due to repetition.

Next, concerning the data after the first repetition, rearrangement of data is performed in accordance with interleaving pattern "10[5[3×2]×2]" in the interleaving section 104. As a result, the data after interleaving becomes {d1, d4, d7, d2, d6, d2, d5, d8, d3, d6}.

Next, the second repetition section 105 performs the second repetition to the data after interleaving in accordance with the processing-flow of FIG. 6. Firstly,

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in ST401 to ST402, in accordance with the above expressions (8) to (9), 'r2' and 'X2' are calculated as follows:

$$r2 = R - r1' = 4 - 2 = 2 \quad (19)$$

$$5 \quad X2 = N1/r2 = 10/2 = 5 \quad (20)$$

Next, in ST403 to ST408, the number of bits of corresponding bits is increased in accordance with the above expression (10) up to the state where 'Ct' becomes 'N1' from '1'. Now, in the case where 'b2' is set to 'b2=2', in accordance with the above expression (10), the number of bits of 'd4' to be data of the second bit as well as the number of bits of 'd5' to be data of the seventh bit are increased, thus the second repetition is performed. Consequently, the data after the second repetition becomes {d1, d4, d4, d7, d2, d6, d2, d5, d5, d8, d3, d6} as showed in FIG. 9.

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since repetition is performed at two stages before and after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame. For that reason, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the conventional coding processing apparatus and the conventional decoding processing apparatus in which repetition is performed

only once before interleaving.

Further, in the above specific example, in the case where the interleaving pattern is $10[5[3 \times 2] \times 2]$, an effect of the present embodiment becomes the most remarkable. However, even though an interleaving pattern is another one, it can be observed that the present embodiment has an effect.

Furthermore, in the above specific example, there is described the embodiment while setting various kinds of parameters arbitrarily. However, it is nothing but one example. Accordingly, the effect of the present embodiment is not observed while being limited from values of these parameters, but the effect of the present embodiment is observed even though parameters adopt another values.

(Embodiment 2)

Next, there will be described an embodiment 2 of the present invention. FIG. 10A is a block diagram illustrating a configuration of a coding processing apparatus according to the embodiment 2 of the present invention. Further, FIG. 10B is a block diagram illustrating a configuration of a decoding processing apparatus according to the embodiment 2 of the present invention. In a coding processing apparatus 800, the configuration of the coding processing apparatus 800 is one in which the second repetition section 105 is removed

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from the coding processing apparatus 100 of the embodiment 1. Another configuration and operation of respective sections are the same as that of coding processing apparatus 100.

5 Consequently, in a transmitter side, the data which is subjected to the error correction coding processing in the error correction coder 102 is subjected to a first repetition by the first repetition section 103 in which 'r1' calculated in ST302 at the processing-flow showed
10 in FIG. 5 described-above is taken to be 'r1=R'. The data after the first repetition is rearranged in the interleaving section 104. Subsequently, the data is subjected to predetermined modulation processing and predetermined radio processing and so forth, before
15 being transmitted from the transmission antenna 107.

On the other hand, in a decoding processing apparatus 810, the configuration of the decoding processing apparatus 810 is one in which the first puncturing section 111 is removed from the decoding
20 processing apparatus 110 of the embodiment 1. Another configuration and operation of respective sections are the same as that of decoding processing apparatus 110.

Consequently, in the receiver side, data to which inverse rearrangement against the interleaving of the
25 transmitter side is performed in the deinterleaving section 112 is subjected to inverse second puncturing against the first repetition in accordance with the

processing-flow showed in FIG. 8 described above by the second puncturing section 113. The data after the second puncturing is subjected to the error correction by Viterbi decoding and so forth in the error correction
5 decoder 114.

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, the repetition is performed while determining increased bits in accordance with the code
10 rate such that in the case where the code rate of the data is '1/2', the increased bits are determined in every the number of bits of multiples of 2, and such that in the case where the code rate of the data is '1/3', the increased bits are determined in every the number of bits
15 of multiples of 3. Consequently, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, it is possible to prevent that the repetition is performed repeatedly to a plurality of data after error correction coding, which
20 are generated from the same data before error correction coding, caused by error correction coding processing. Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since it is possible to enhance an effect
25 of the error correction coding, it is possible to improve a bit error rate characteristic when the receiver side performs error correction in comparison with the

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conventional coding processing apparatus and the conventional decoding processing apparatus.

(Embodiment 3)

5 Next, there will be described an embodiment 3 of the present invention. FIG. 11A is a block diagram illustrating a configuration of a coding processing apparatus according to an embodiment 3 of the present invention. Further, FIG. 11B is a block diagram
10 illustrating a configuration of a decoding processing apparatus according to the embodiment 3 of the present invention.

 In a coding processing apparatus 900, the configuration of the coding processing apparatus is one
15 in which the first repetition section 103 is removed from the coding processing apparatus 100 of the first embodiment. Another configuration and operation of respective sections are the same as that of the coding processing apparatus 100.

20 Consequently, in the transmitter side, the data which is rearranged in the interleaving section 104 is subjected to a second repetition by the second repetition section 105 in which 'r2' calculated in ST401 at the processing flow showed in FIG. 6 described-above is taken
25 to be 'r2=R'. The data after the second repetition is subjected to predetermined modulation processing and predetermined radio processing and so forth, before

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On the other hand, in a decoding processing apparatus 910, the configuration is one in which the second puncturing section 113 is removed from the decoding processing apparatus 110 of the embodiment 1. Another configuration and operation of respective sections are the same as that of the decoding-coding processing apparatus 110.

Thus, according to the coding processing apparatus and the decoding processing apparatus of the present embodiment, since the repetition is performed after interleaving, it is possible to prevent that the bits increased due to repetition exist while being partial to one position within a frame. Consequently, according to the coding processing apparatus and the decoding

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invention, it is possible to scheme improvement of communication quality because resistibility to a burst error in a propagation path becomes high.

This application is based on the Japanese Patent
5 Application No.HEI11-092078 filed on March 31, 1999,
entire content of which is expressly incorporated by
reference herein.

Industrial Applicability

10 The present invention is applicable to a base
station apparatus employed in a radio communication
system and/or a communication terminal apparatus such
as a mobile station performing radio communication
between the base station apparatus and the mobile
15 station.

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